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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,445	09/07/2004	Axel Hulsmann	08788.0036USWO	5325
23552	7590	09/08/2005	EXAMINER	
MERCHANT & GOULD PC P.O. BOX 2903 MINNEAPOLIS, MN 55402-0903			ARENA, ANDREW OWENS	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/502,445

Applicant(s)

HULSMANN, AXEL

Examiner

Andrew O. Arena

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 July 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION*****Claim Objections***

1. Claim 1 is objected to because of the following informalities: the word "multiplayer" should be replaced with "multilayer".

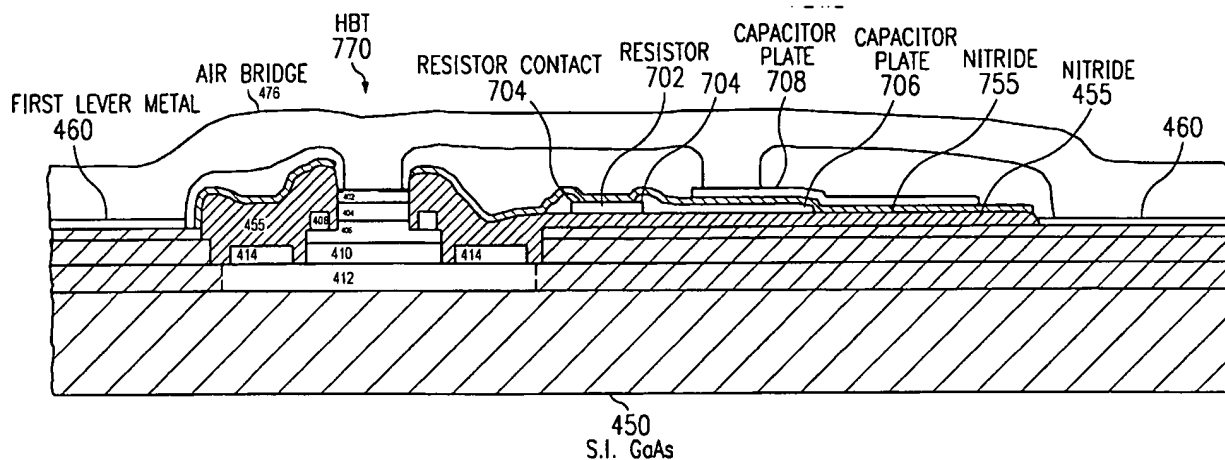
***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hill (US 6, 028, 348), hereinafter Hill.
3. All rejections made in this office action based on Hill refer to Fig 7, which includes the structure of Fig 4L (col 8, ln 16-17). A copy of Hill Fig 7 including the reference numerals from Fig 4L is shown below.



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4. Regarding claim 1, Hill discloses an integrated circuit arrangement (col 8 ln 16-18) on the basis of III/V semiconductors (col 3 ln 22), comprising at least one active component (770; col 8 ln 17) and a multilayer configuration of wiring levels (414, 460, 704, 706, 708; col 7 ln 65, col 8 ln 5, 8) characterized in that a metallization layer comprising a metal contact (414; col 4 ln 27) of the at least one active component is formed to be a lower one of the wiring levels (414 is a wiring level: Fig 4L, also 4M).

5. Regarding claim 9, Hill discloses the integrated circuit arrangement as claimed in claim 1, characterized in that the at least one active semiconductor component (770) is a transistor (col 8 ln 17, col 3 ln 14-15) and a metal contact (414) of the collector (col 4 ln 27) of the transistor is formed by means of the metallization layer.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hill.

8. Regarding claim 3, Hill discloses the integrated circuit arrangement as claimed in claim 1, characterized that an electric resistor is formed in a wiring level (704) by means of an interruption (702; col 7 ln 61) in the metallization layer. Hill does not disclose this resistor is formed in the lower wiring level. However, such difference is regarded as

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nothing more than an obvious design choice. That is, varying parameters such as circuit connections and the location of the resistor in the integrated circuit merely requires routine experimentation. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to adjust the location of the resistor to the lower wiring level.

9. Claims 2 and 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hill in view of Ko et al. (US 2001/0053840), hereinafter Ko.

10. Regarding claim 2, Hill discloses the integrated circuit arrangement as claimed in claim 1, characterized in that a passivation layer (455; col 4 ln 41) is applied on the metallization layer of the at least one active component (455 is on 414), but does not disclose the passivation layer made of a material which has a small relative dielectric constant ( $\epsilon_{r1} < 3$ ). Ko is analogous art that teaches a small dielectric constant below 3 is preferred ([0005] ln 8-14, [0007] ln 18). The field of endeavor is monolithic microwave integrated circuits for both Hill (col 3 ln 5-10) and Ko ([0032] ln 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to form the dielectric (455) of Hill out of a low-dielectric-constant material as taught by Ko; for at least the purpose of increased IC operating speed ([0006] ln 11-13).

11. Regarding claim 4, Hill discloses that a central wiring level (702+704+706; col 7 ln 60-65) is disposed above the passivation layer (455) and covered by another passivation layer (755; col 8 ln 5-6) made of a material which has a mean relative dielectric constant  $\epsilon_{r2}$  ( $\epsilon_{r2} > \epsilon_{r1}$ , preferably  $\epsilon_{r2} \approx 7$ ). Hill inherently meets the limitation

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of the claim, since it discloses the passivation layer material is silicon nitride; which is known in the art to have a dielectric constant larger than 3 of about 7 (see the entry for silicon nitride on <http://www.semiconductor glossary.com>, for example).

12. Regarding claim 5, Hill discloses that an upper wiring level (708, 476; col 8 ln 8, col 5 ln 12) is disposed above the central passivation layer.

13. Regarding claim 6, Hill discloses that a capacitive component (706+755+708; col 7 ln 65, col 8 ln 5-9) is formed by means of a section (706) of the central wiring level and a section (708) of the upper wiring level.

14. Regarding claim 7, Hill discloses that the upper wiring level is formed of metal (col 5 ln 10-13, col 8 ln 8). The limitation "formed by galvanic deposition" is a product-by-process limitation and has not been given patentable weight. The case law establishing this precedent follows:

"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

15. Regarding claim 8, Hill discloses that the upper wiring level is constructed at least partly by air bridge technology (col 5 ln 10-13).

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hill in view of Ko as applied to claim 4 above, and further in view of Baba et al. (US 6,853,054), hereinafter Baba.

17. Regarding claim 10, Hill discloses the integrated circuit arrangement as claimed in claim 5, but does not disclose expressly that at least one microstrip conductor is

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formed by means of the lower, the central, and the upper wiring levels. Baba is analogous art that discloses at least one microstrip conductor (16+18 and 20+18; col 5 ln 10, col 5 ln 15-17) formed by means of the various wiring levels (Baba uses the terms transmission line and microstrip interchangeably for a wiring layer adjacent to a grounded layer: col 1 ln 38-40, col 1 67, col 2 ln 1, col 4 ln 24-29). The field of endeavor is MMICs with a multilayer wiring structure for both Hill (col 3 ln 5-10) and Baba (col 3 ln 51, col 5 ln 10). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to provide the multilayer wiring structure of Hill with a microstrip conductor as taught by Baba; for at least the purpose of stabilizing transmission characteristics (col 5 ln 17-18).

18. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hill in view of Shimamoto et al. (US 6,683,260), hereinafter Shimamoto.

19. Regarding claim 11, Hill discloses the integrated circuit arrangement as claimed in claim 1, but does not expressly disclose a waveguide. Shimamoto is analogous art that discloses (Fig 1A) a waveguide (col 6 ln 49-50). The field of endeavor is multilayer wiring structures including transmission lines for both Hill (414, 460, 704, 706, 708) and Shimamoto (col 4 ln 53-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to provide the multi-layer wiring structure of Hill with the waveguide structure taught by Shimamoto (Fig 1A, 3a&3b+5b); for at least the purpose of excellent transmission characteristics (Shimamoto: col 8 ln 45-48).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven Loke  
Primary Examiner  
